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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/009,649	05/29/2002	Martin Vorbach	2885/56	8424

26646 7590 04/30/2008

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EXAMINER	
DAO, THUY CHAN	
ART UNIT	**PAPER NUMBER**
2192	
MAIL DATE	**DELIVERY MODE**
04/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/009,649	VORBACH ET AL.	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *179-181 and 183-203* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *179-181 and 183-203* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/04/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on February 4, 2008 has been entered.

2. Claims 179-181 and 183-203 have been examined.

Information Disclosure Statement

3. The Office acknowledges receipt of the Information Disclosure Statement filed on February 4, 2008. It has been placed in the application file and the information referred to therein has been considered by the examiner.

Response to Amendments

4. Per Applicants' request, claims 179-181, 183-185, 189, and 203 have been amended.

Specification

5. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

Claim Objections

6. Claim 203 is objected to because of minor informalities: the last two lines are missing. The examiner respectfully requests the Applicants, in the next communication with the Office, submit the claim listing commenced in separate sheets.

Response to Arguments

7. Applicants' arguments have been fully considered.

a) Rejections of claims 179, 181, 185, 187, and 188 under 35 USC 102(e) in view of Cooke (Remarks, pp. 7-8):

The examiner respectfully disagrees with Applicants' assertions. Cooke explicitly teaches *a method for programming a system having a cellular structure* (e.g., col.5: 31-41)*, comprising:*

extracting a control flow graph of a program (e.g., col.2: 60-64; col.6: 45-48)*;*

separating the control flow graph into a plurality of subgraphs (e.g., col.4: 17-43, mapping a basic unit of code to an Application Specific Integrated Circuit ASIC; col.5: 31-41, independent subgraph are packed onto a singe ASIC; col.6: 1-21, after graph is partitioned, each block may be viewed as a single task)*; and*

distributing the plurality of subgraphs among a plurality of programmable hardware modules (e.g., col.5: 12-49; col.6: 9-34 and 38-64);

wherein the separation step includes separating the control flow graph so as to minimize connections between the plurality of subgraphs (e.g., col.4: 17-28; col.5: 31-41, no connections between the plurality of independent subgraphs; col.6: 9-18).

b) Rejections of claim 179 under 35 USC 102(e) in view of Henzinger (Remarks, pp. 7-8):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

c) Rejections of claims 190-193 under 35 USC 102(e) in view of Kessler (Remarks, pp. 9-10):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

d) Rejections of claims 194-202 under 35 USC 102(e) in view of Getzinger (Remarks, pp. 10-11):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

e) Rejections of claim 194 under 35 USC 102(e) in view of Lisitsa (Remarks, pp. 11-12):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

f) Rejections of claim 180 under 35 USC 103(a) in view of Campbell further in view of Beckerle (Remarks, pp. 12-13):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

g) Rejections of claims 183, 184, and 186 under 35 USC 103(a) in view of Cooke further in view of Wuytack (Remarks, pp. 13-14):

Claims 183, 184, and 186 depend from claim 181 and therefore include all of the features recited in claim 181. Accordingly, the examiner respectfully maintains the combination of Cooke and Wuytack renders unpatentable these dependent claims for the same reasons set forth above in (a).

h) Rejections of claim 189 under 35 USC 103(a) in view of Cooke further in view of Maslennikov (Remarks, page 14):

Claim 189 depends from claim 181 and therefore include all of the features recited in claim 181. Accordingly, the examiner respectfully maintains the

combination of Cooke and Maslennikov renders unpatentable this dependent claim for the same reasons set forth above in (a).

i) Rejections of claim 203 under 35 USC 103(a) in view of Cooke further in view of Wuytack (Remarks, pp. 14-15):

Applicants' arguments have been considered but are moot in view of the new ground of rejection as applied in details below.

Claim Rejections – 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 180 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,418,953 to Hunt et al. (art made of record, hereinafter "Hunt").

Claim 180:

Hunt discloses *a method for programming a system having a cellular structure* (e.g., col.1: 32-48; FIG. 3, col.8: 34-64)*, comprising:*

extracting a data flow graph of a program (e.g., FIG. 1, col.4: 41-64)*;*

separating the data flow graph into a plurality of subgraphs (e.g., FIG. 3, subgraph execution programs SEPs, col.4: 65 – col.5: 6; col.8: 34-64)*,*

so as to minimize connections between the plurality of subgraphs (e.g., col.5: 51-60; col.6: 36-59; col.9: 4-17)*, and*

distributing the plurality of subgraphs among a plurality of hardware modules (e.g., FIG. 3, col.8: 34-64; col.6: 65 – col.7: 13)*.*

9. Claims 190-193 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,327,125 to Iwase et al. (art made of record, hereinafter "Iwase").

Claim 190:

Iwase discloses *a method of executing a single program on a system having an array of runtime reconfigurable cells, comprising:*

transmitting a data signal from a first cell to a second cell (e.g., FIG. 2, col.9: 44-58; col.13: 26-36) *and*

transmitting a status with the data signal, the status indicating whether the data signal is valid (e.g., FIG. 7, col.13: 37-51; col.13: 67 – col.14: 4; col.14: 12-34).

Claim 191:

The rejection of base claim 190 is incorporated. Iwase also discloses *receiving a valid data signal at the second cell and acknowledging receipt of the valid data signal* (e.g., col.15: 16-49).

Claim 192:

The rejection of base claim 190 is incorporated. Iwase also discloses *transmitting by the second cell an indication that a signal is expected* (e.g., FIG. 2, col.9: 44-58; col.13: 26-36).

Claim 193:

The rejection of base claim 190 is incorporated. Iwase also discloses *transmitting by the first cell an indication that the first cell is transmitting the expected signal* (e.g., col.15: 40-66; col.12: 11-27).

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 179, 181, 185, and 187-188 are rejected under 35 U.S.C. 102(e) as being anticipated by Cooke (art of record, US Patent No. 5,966,534).

Claim 179:

Cooke discloses *a method for programming a system having a cellular structure* (e.g., col.5: 31-41)*, comprising:*

extracting a control flow graph of a program (e.g., col.2: 60-64; col.6: 45-48)*;*

separating the control flow graph into a plurality of subgraphs (e.g., col.4: 17-43, mapping a basic unit of code to an Application Specific Integrated Circuit ASIC; col.5: 31-41, independent subgraph are packed onto a singe ASIC; col.6: 1-21, after graph is partitioned, each block may be viewed as a single task)*; and*

distributing the plurality of subgraphs among a plurality of programmable hardware modules (e.g., col.5: 12-49; col.6; 9-34 and 38-64);

wherein the separation step includes separating the control flow graph so as to minimize connections between the plurality of subgraphs (e.g., col.4: 17-28; col.5: 31-41, no connections between the plurality of independent subgraphs; col.6: 9-18).

Claim 181:

Cooke discloses *a method for programming a system having a cellular structure, comprising:*

extracting from a program at least one of a data flow graph and a control flow graph (e.g., col.2: 60-64; col.6: 45-48)*;*

separating the at least one of the graphs into a plurality of subgraphs (e.g., col.3: 63-66; col.4: 17-43; col.5: 31-41; col.2: 25-29; col.3: 23-26; col.6: 1-21)*; and*

distributing the plurality of subgraphs among a plurality of hardware modules (e.g., col.3: 18-26; col.5: 12-49; col.6: 9-34 and 38-64);

wherein the separation step includes separating the at least one of the graphs so as to minimize connections between the plurality of subgraphs (e.g., col.5: 31-41, no connections between the plurality of independent subgraphs; col.6: 9-18).

Claim 185:

The rejection of base claim 181 is incorporated. Cooke also discloses *the separating step includes separating the at least one of the graphs into the plurality of subgraphs so that the subgraphs match resources of the hardware modules* (e.g., col.5: 16-24; col.6: 38-45).

Claim 187:

The rejection of base claim 181 is incorporated. Cooke also discloses *each of the plurality of subgraphs includes nodes, the method further comprising transmitting status signals between nodes within one of the subgraphs so that a state of each individual one of the nodes of the one of the subgraphs is available to each of the other nodes of the one of the subgraphs* (e.g., col.5: 50 – col.6: 8).

Claim 188:

The rejection of base claim 181 is incorporated. Cooke also discloses *each of the plurality of subgraphs includes nodes, the method further comprising transmitting status signals from a first node of at least one of the plurality of subgraphs to a higher-level unit adapted to control configuration of the plurality of hardware modules so as to trigger reconfiguration* (e.g., col.5: 50 – col.6: 8).

12. Claims 194-202 are rejected under 35 U.S.C. 102(e) as being anticipated by Getzinger (art of record, US Patent No. 4,972,314).

Claim 194:

Getzinger discloses *a method of executing a program on a runtime reconfigurable array of cells* (e.g., FIG. 1, Parallel Processing Concept with 16 Arithmetic Processors 1-16, col.5: 64 – col.6: 14)*, the method comprising:*

forming a plurality of subgraphs based on a program (e.g.,

FIG. 1, Graph Process Controller, col.4: 63-67; a plurality of subgraphs as node structures, col.9: 37-48;

node instances (subgraph instances) are ready to "independently and concurrently" executed by placing them on a dispatch queue, col.11: 60-67 and col.1: 52-59;

nodes (subgraphs) are scheduled and dispatched to 16 Arithmetic Processors AP 1-16, col.16: 65 – col.17:21 and FIG. 1)*;*

computing a first part of a first one of the subgraphs with a first cell (e.g., FIG. 5, Graph {A, B, C}, first subgraph as {A, C}, second subgraph as {B}, col.9: 36-62; first part A of first subgraph {A, C} computed with a first Arithmetic Processor AP 1)*;*

after the computing, reconfiguring the first cell for computation of a first part of a second one of the subgraphs (e.g., FIG. 5, after the computing, reconfiguring AP 1 for computation first part B of second subgraph {B}, please see Node A output source to 2, 2 sink to B, B assigned to AP 1)*; and*

simultaneously with the reconfiguring, computing a second part of the first subgraph with a second cell (e.g., FIG. 5, simultaneously, computing second part C of first subgraph {A, C} with a second Arithmetic Processor AP 2, please see more in FIG. 3 with Dispatch Queue, Arithmetic Processors (in the instant case: 2 APs), Graph Process Controller GPC Scheduler, col.11: 60 - col.12: 29).

Claim 195:

The rejection of base claim 194 is incorporated. Getzinger also discloses *storing configurations for the first one of the subgraphs and the second one of the subgraphs configuration registers associated with the first cell* (e.g., FIG. 9, Graphic Processor Memory GPM, col.17: 22 - 59).

Claim 196:

The rejection of intervening claim 195 is incorporated. Getzinger also discloses *marking unconfigured ones the configuration registers as unconfigured* (e.g., col.28: 48 – col.29: 36).

Claim 197:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by the cell structure* (e.g., FIG. 3, col.11: 60 – col.12: 30).

Claim 198:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by a higher-level loading unit* (e.g., FIG. 2, col.7: 22 – col.8: 29).

Claim 199:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on an externally generated status signal* (e.g., FIG. 2, col.7: 22 – col.8: 29).

Claim 200:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell as a function of a present configuration of the first cell and a received status signal* (e.g., FIG. 3, col.11: 60 – col.12: 30).

Claim 201:

The rejection of base claim 194 is incorporated. Getzinger also discloses:

activating an unconfigured configuration register in the first cell (e.g., col.28: 48 – col.29: 36)*;*

requesting a configuration from a higher-level load unit when the unconfigured configuration register is activated (e.g., col.7: 22 – col.8: 29)*; and*

suspending execution of a subgraph until the requested configuration is fully loaded (e.g., FIG. 7, Graph Process Controller Functions, col.14: 31-66).

Claim 202:

The rejection of base claim 194 is incorporated. Getzinger also discloses *triggering a loading of a configuration of the first cell when a status signal generated by the cell structure received by the first cell* (e.g., col.9: 11-28).

Claim Rejections – 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 183-184 and 186 are rejected under 35 U.S.C. 103(a) as being unpatentable by Cooke in view of Wuytack (art of record, US Patent No. 6,421,809).

Claim 183:

The rejection of base claim 181 is incorporated. Cooke does not explicitly disclose *the separating step includes separating the at least one the graphs into the*

plurality of subgraphs so that data transmission between the plurality of subgraphs is minimized.

However, in an analogous art of parallel processing optimization (e.g., col.3: 2-8), Wuytack further discloses *the separating step includes separating the at least one the graphs into the plurality of subgraphs so that data transmission between the plurality of subgraphs is minimized* (e.g., col.7: 26-35; col.8: 24-32).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Wuytack into that of Cooke. One would have been motivated to do so to enhance the Cooke's method and optimize memory organization and data parallel access capabilities as suggested by Wuytack (e.g., col.2: 53 – col.3: 28).

Claim 184:

The rejection of base claim 181 is incorporated. Wuytack further discloses *the separating step includes separating the at least one of the graphs into the plurality of subgraphs so that no loop-back is obtained between the plurality of subgraphs* (e.g., col.14: 31-41; col.22: 6-27).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Wuytack into that of Cooke. One would have been motivated to do so as set forth above.

Claim 186:

The rejection of base claim 181 is incorporated. Wuytack further discloses *inserting memory elements between the plurality subgraphs, the memory elements adapted to save data passed between subgraphs* (e.g., col.3: 8-29; col.9: 66 – col.10: 14).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Wuytack into that of Cooke. One would have been motivated to do so as set forth above.

15. Claim 189 is rejected under 35 U.S.C. 103(a) as being unpatentable by Cooke in view of Maslennikov (art of record, US Patent No. 6,301,706).

Claim 189:

The rejection of base claim 181 is incorporated. Cooke does not explicitly disclose *the extracting step includes, for a conditional instruction, extracting a plurality of different subgraphs, each representing a different instruction path, one of the different subgraphs being executed depending on an evaluation of the conditional instruction.*

However, in an analogous art of optimizing parallel processing architectures (e.g., col.2: 13-16), Maslennikov discloses the extracting step includes, for a conditional instruction, extracting a plurality of different subgraphs, each representing a different instruction path, one of the different subgraphs being executed depending on an evaluation of the conditional instruction (e.g., col.2: 36-58).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teachings of Maslennikov into that of Cooke. One would have been motivated to do so to enhance the Cooke's system and reduce redundant speculative computations in the loop body as suggested by Maslennikov (e.g., col.2: 1-10).

16. Claim 203 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,537,580 to Giomi et al. (art made of record, hereinafter "Giomi") in view of US Patent No. 6,438,747 to Schreiber et al. (art made of record, hereinafter "Schreiber").

Claim 203:

Giomi discloses *a method for programming a system, comprising:*

extracting from a program at least one of a data flow graph and a control flow graph (e.g., col.2: 34-46; col.5: 33-44)*;*

separating the at least one of the graphs into a plurality of subgraphs (e.g., col.5: 18-44; FIG. 5, 'VALUE" "NET" "IF" "CASE" nodes as subgraphs)*; and*

distributing the plurality of subgraphs among a plurality of hardware modules (e.g., col.2: 33-46; col.6: 19-28)

wherein: the extracting includes, for a conditional instruction of the program, extracting a plurality of different subgraphs, each representing a different instruction path of the conditional instruction, the conditional instruction indicating which of the executed instruction paths is to be selected for providing output of the selected instruction path output to a further subgraph (e.g., FIG. 5, conditional instructions as "IF" "CASE" "LOOP", col.5: 18-44; col.10: 12-24)*; and*

for each one of the different subgraphs, the system sets execution of the subgraph to be bypassed as soon as an evaluation in accordance with the conditional instruction reveals that output of the subgraph will not be selected (e.g., FIG. 5, col.10: 5-12; returning list of Evaluated Conditions and branching to appropriate nodes such as "Net Node" 78 with Expression G 86, please see more in FIG. 6, Get Expression of the Net:G, col.10: 52-58).

Giomi discloses distributing subgraphs as control nodes "IF", "CASE", "LOOP" among a plurality of hardware modules but does not explicitly disclose distributing said subgraphs in *a system having a cellular structure.*

However, in an analogous art, Schreiber further discloses distributing said subgraphs (such as "LOOP") in *a system having a cellular structure* (e.g., col.4: 11-18; col.1: 21-54).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Schreiber's teaching into Giomi's teaching. One would have been motivated to do so to optimize the processing of the loop nest by converting the loop nest code to parallel processes that can be executed concurrently as suggested by Schreiber (e.g., col.1: 21-54).

Conclusion

17. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570,

respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T Dao/

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192